Q.P. Code: 16EC410 **R16**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech II Year II Semester Supplementary Examinations October-2020

PULSE & DIGITAL CIRCUITS

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	**a**	Prove that a low pass circuit acts as an integrator.	**6M**
	b	Design high pass RC circuit for sinusoidal input.	**6M**
		OR	
2	**a**	Design high pass RC circuit for sinusoidal input. [6M]	**6M**
	b	Define clamper. With the help of neat circuit diagrams and output waveforms, Explain the working of positive peak and negative peak clamping circuits.	**6M**

UNIT-II

3	**a**	Elaborate about piece-wise linear approximation for a semiconductor diode characteristics.	**8M**
	b	Explain the working of transistor as a switch and draw the output characteristics	**4M**
		OR	
4		Discuss the operation of collector coupled monostable multivibrator with its output waveforms.	**12M**

UNIT-III

5	**a**	Explain the working of Transistor Miller sweep circuit.	**6M**
	b	What are the advantages of a miller circuit over Bootstrap sweep circuits?	**6M**
		OR	
6	**a**	What are the techniques used to improve the Linearity of current sweeps?	**5M**
	b	Discuss about Transistor Current Time Base Generator.	**7M**

UNIT-IV

7	**a**	Explain about unidirectional diode sampling gate.	**6M**
	b	Write advantages and Disadvantages of sampling gate	**6M**
		OR	
8	**a**	With the help of neat diagram explain the working of a four diode sampling gate.	**6M**
	b	Derive expressions for the gain (A) and Vmin of a four diode sampling gate.	**6M**

UNIT-V

9	**a**	Construct a neat diagram of OR, AND & NOT gates using diodes.	**8M**
	b	Explain the concepts of Open collector	**4M**
		OR	
10		With reference to logic gates explain the terms: (i) Fan out (ii) Noise margin (iii) Propagation delay (iv) Figure of Merit	**12M**

*** END ***